Heterogeneous integration of III-V and silicon devices for digital VLSI

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Agenda

- Microprocessor core and I/O speeds
- Electrical I/O
- Intel's optoelectronics research at universities
- III-V and optical interconnects
- Conclusions
- Acknowledgements

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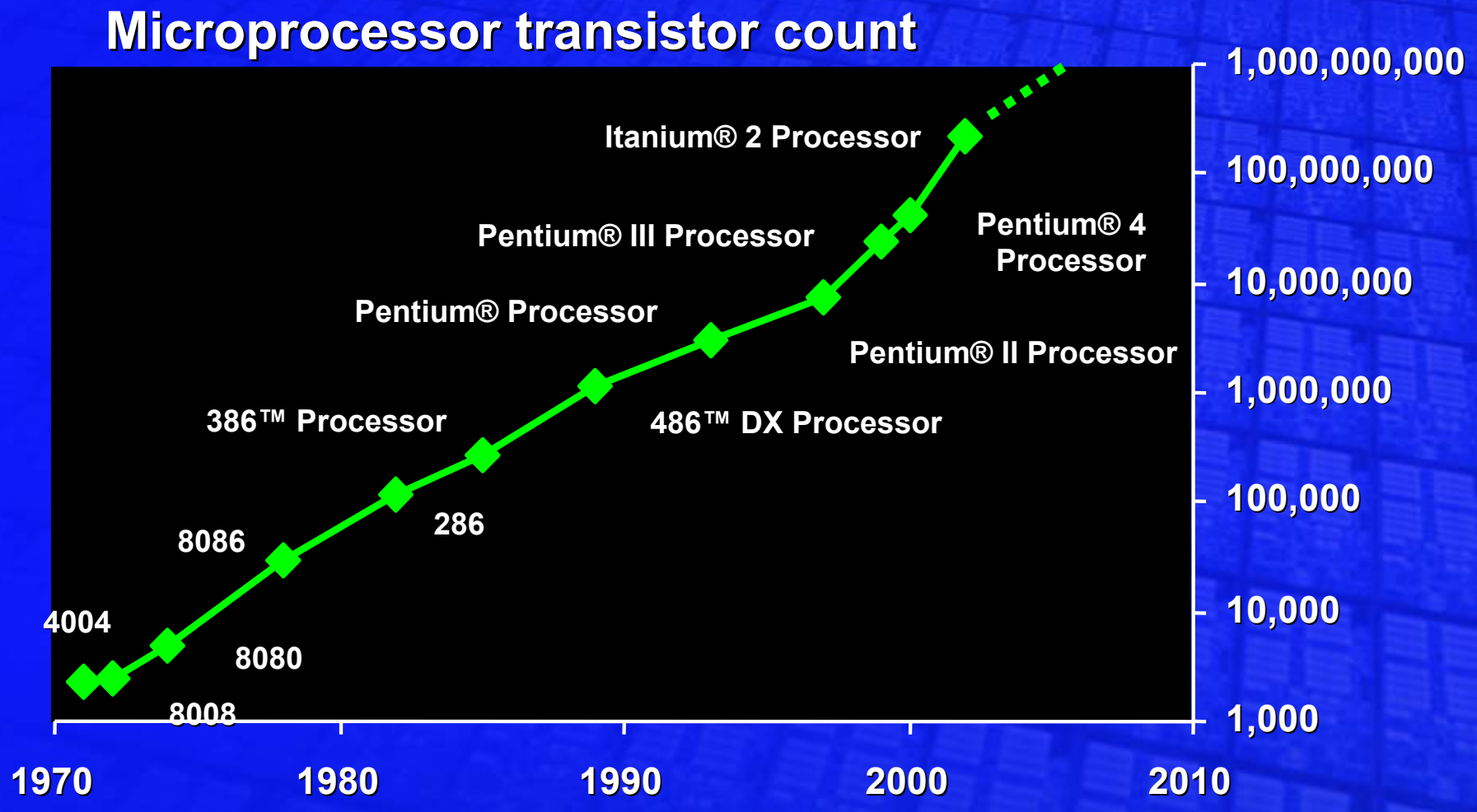
- Backup

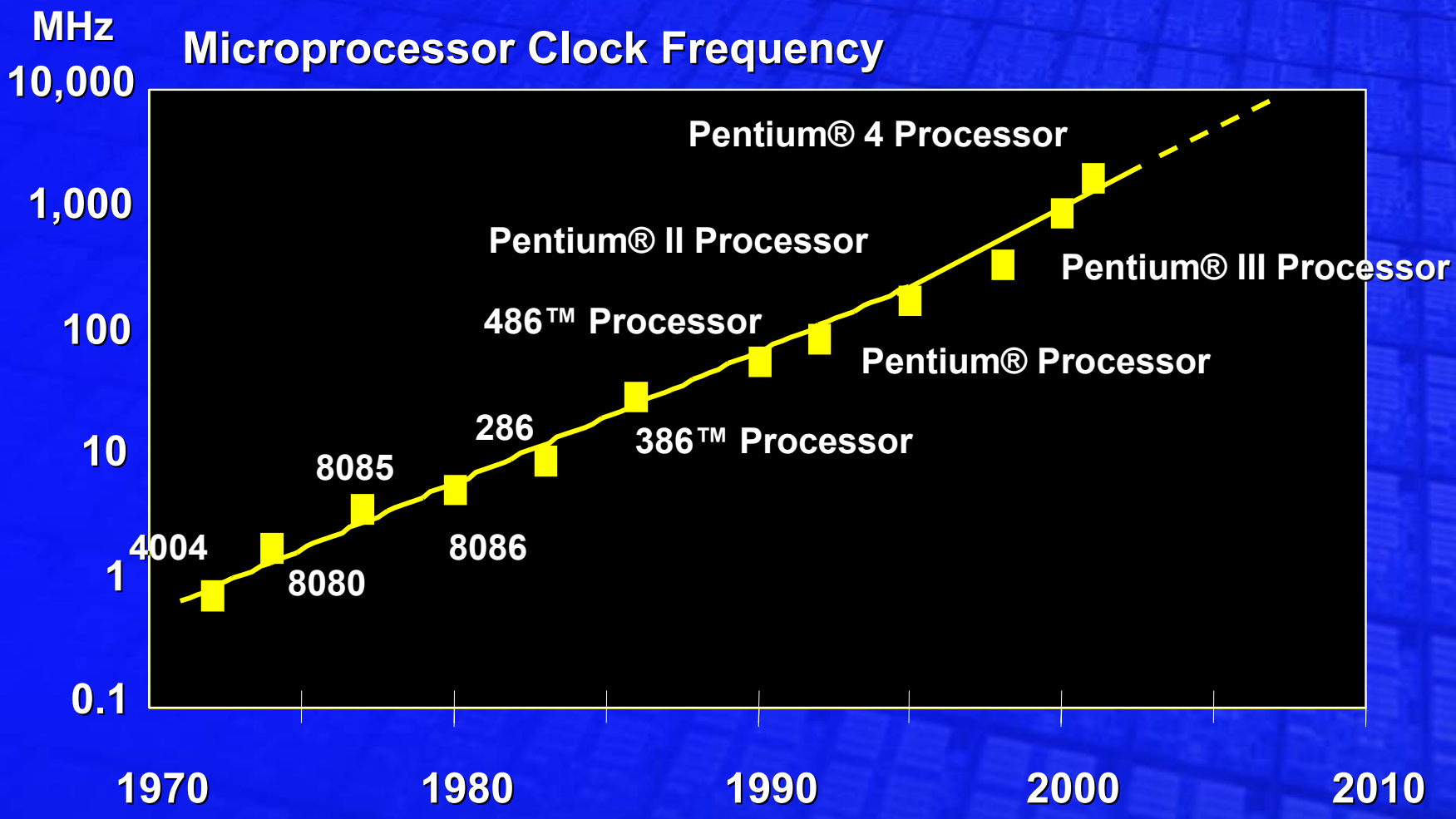
More Transistors per Chip



~ 1B transistor microprocessor by 2007

Source: Intel

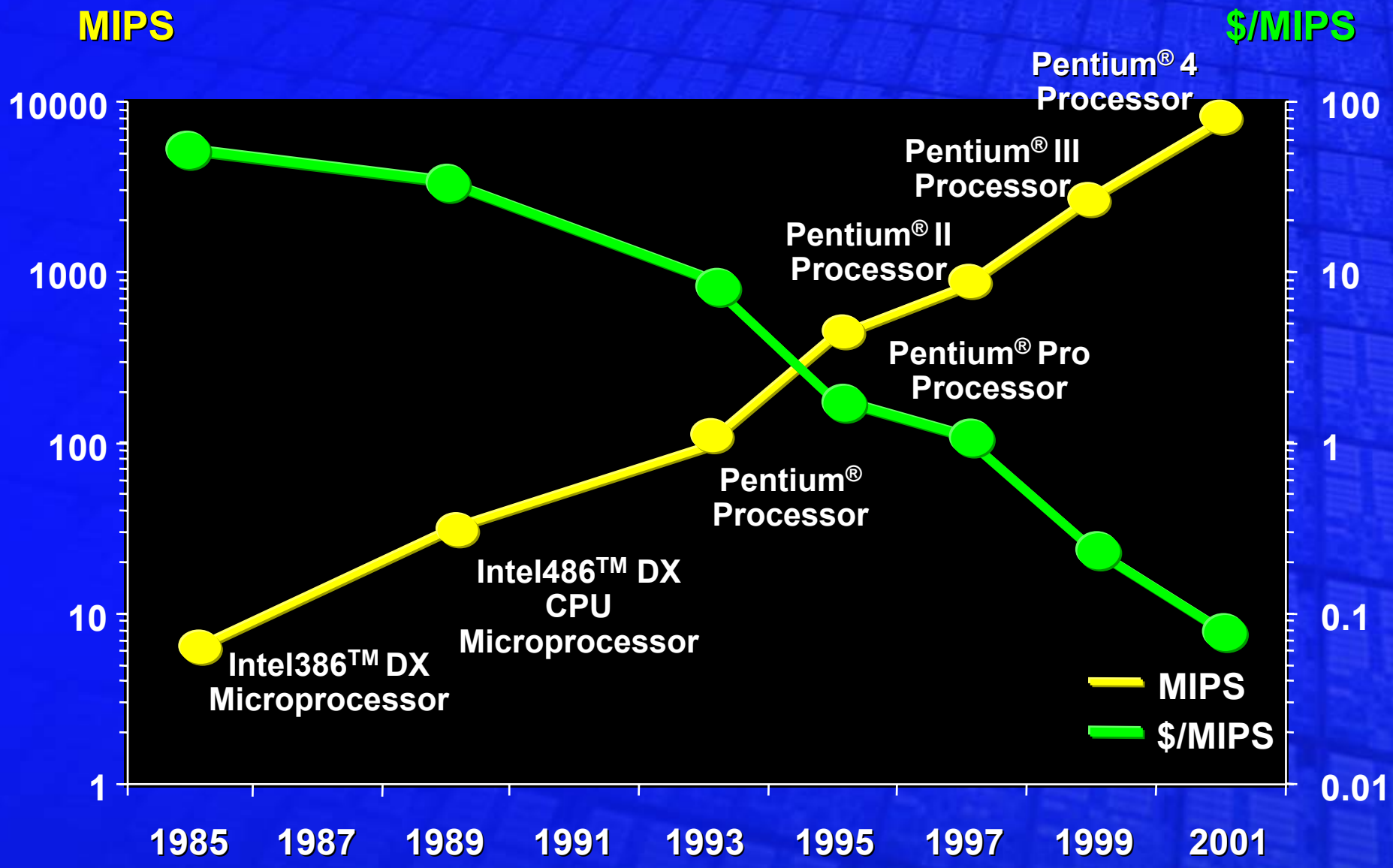
Faster Devices



Microprocessor clock frequency trending to ~ 10GHz by 2007

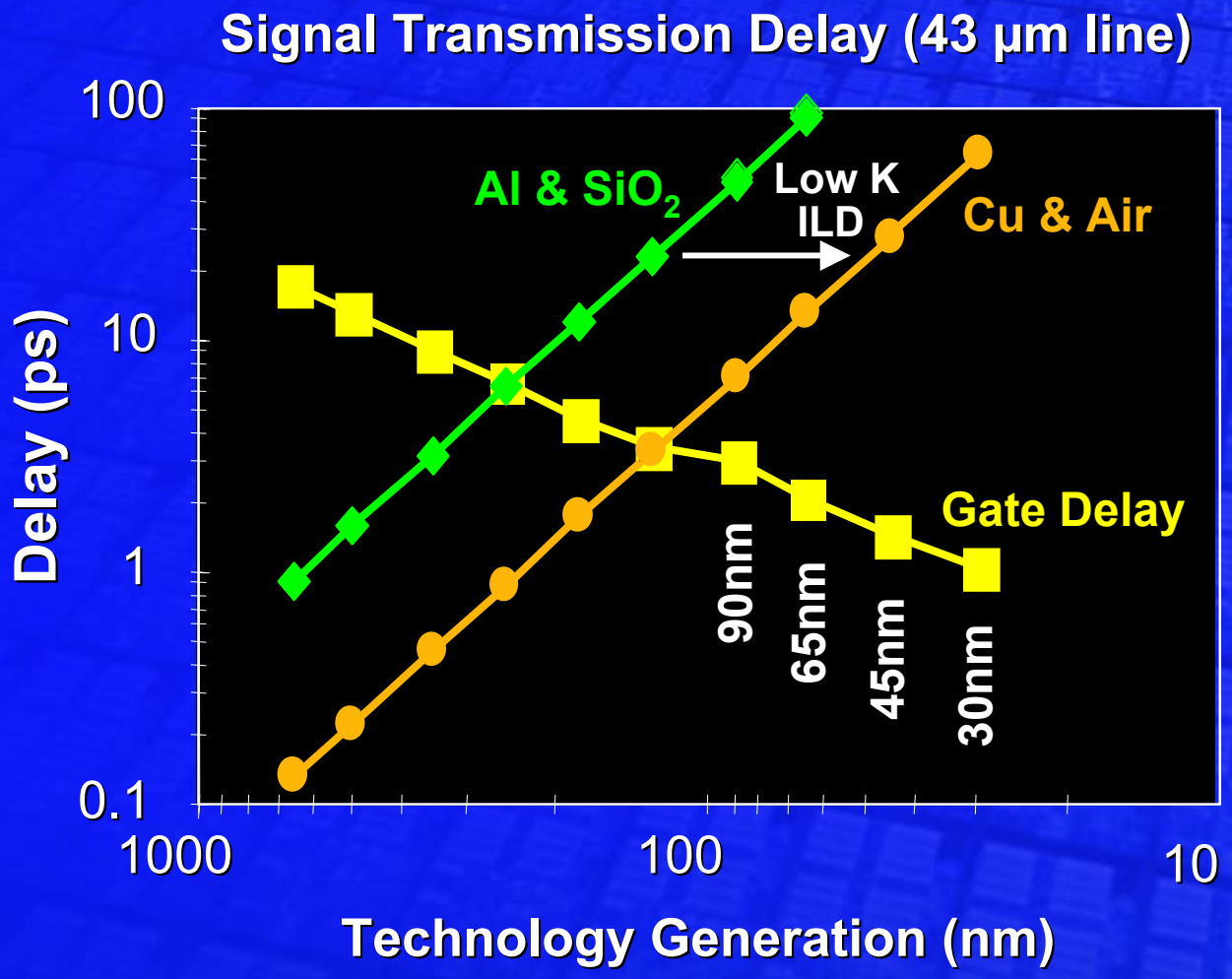
Source: Intel

Higher Performance, Lower Cost



Source: Intel

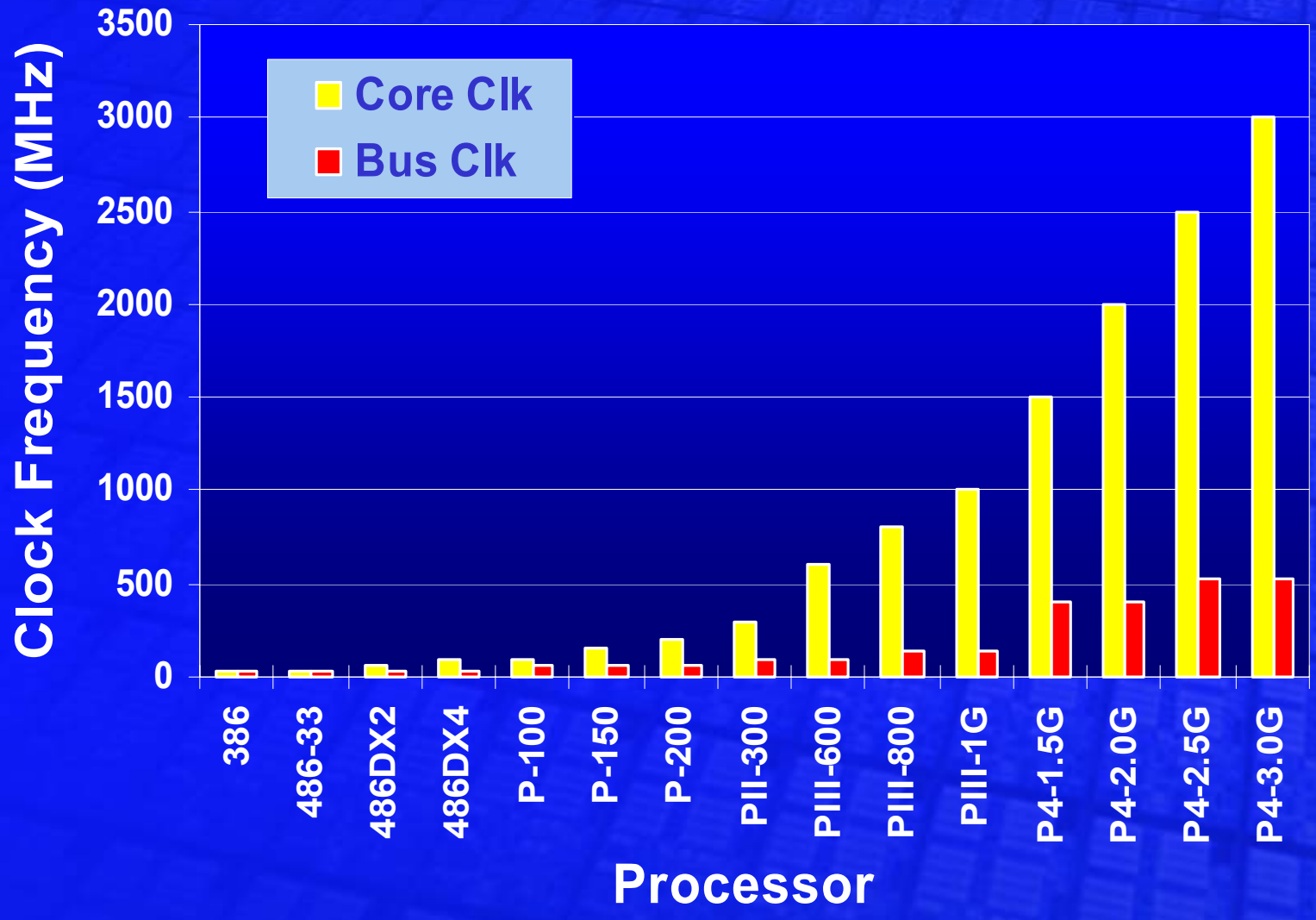
Interconnect Delay Challenge



Need process, circuit design and architectural innovations

Source: Intel

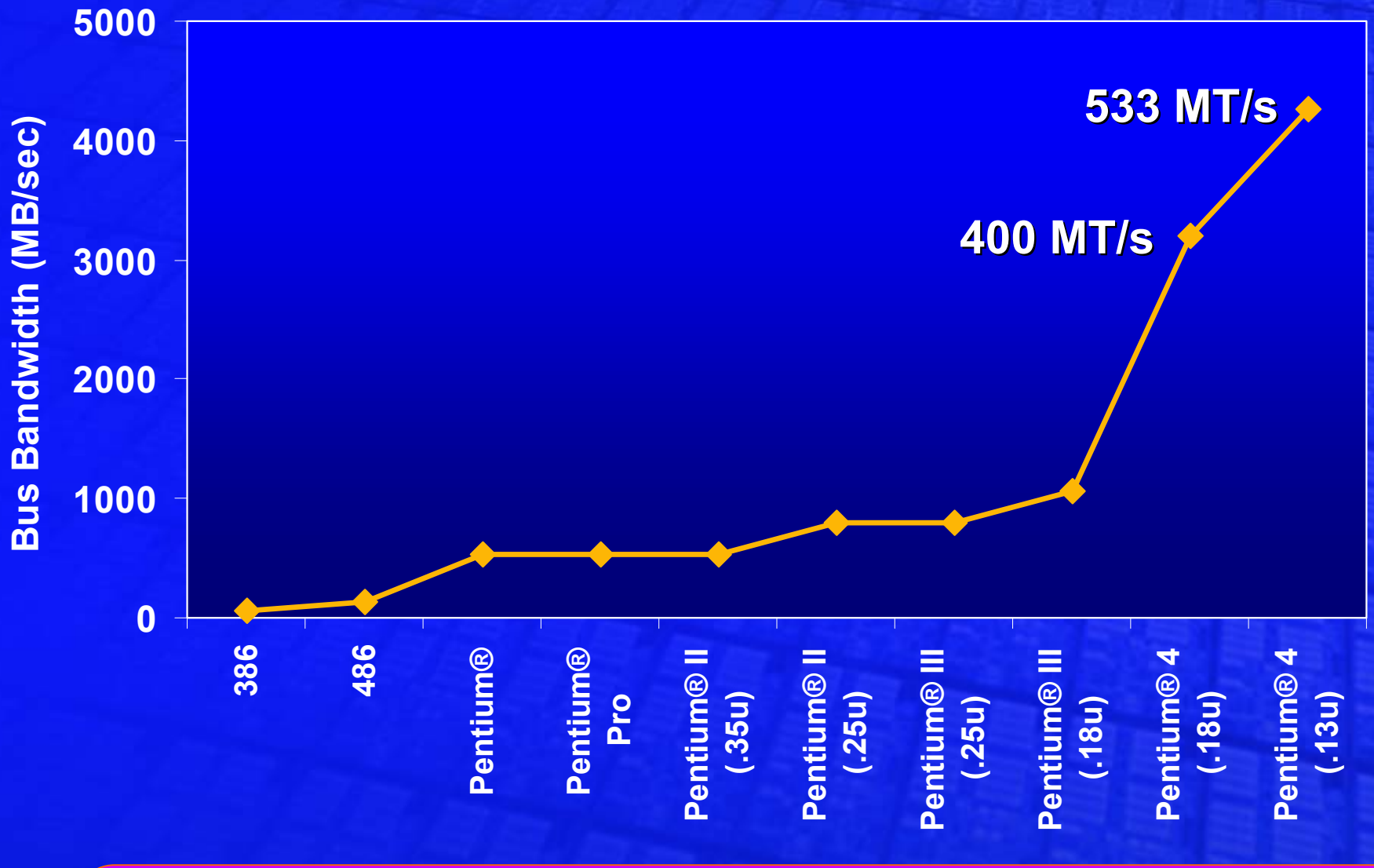
Processor Core Vs. Bus Clock



Bus frequency is not keeping up with the processor core

Bus Bandwidth Trend

K Bytes

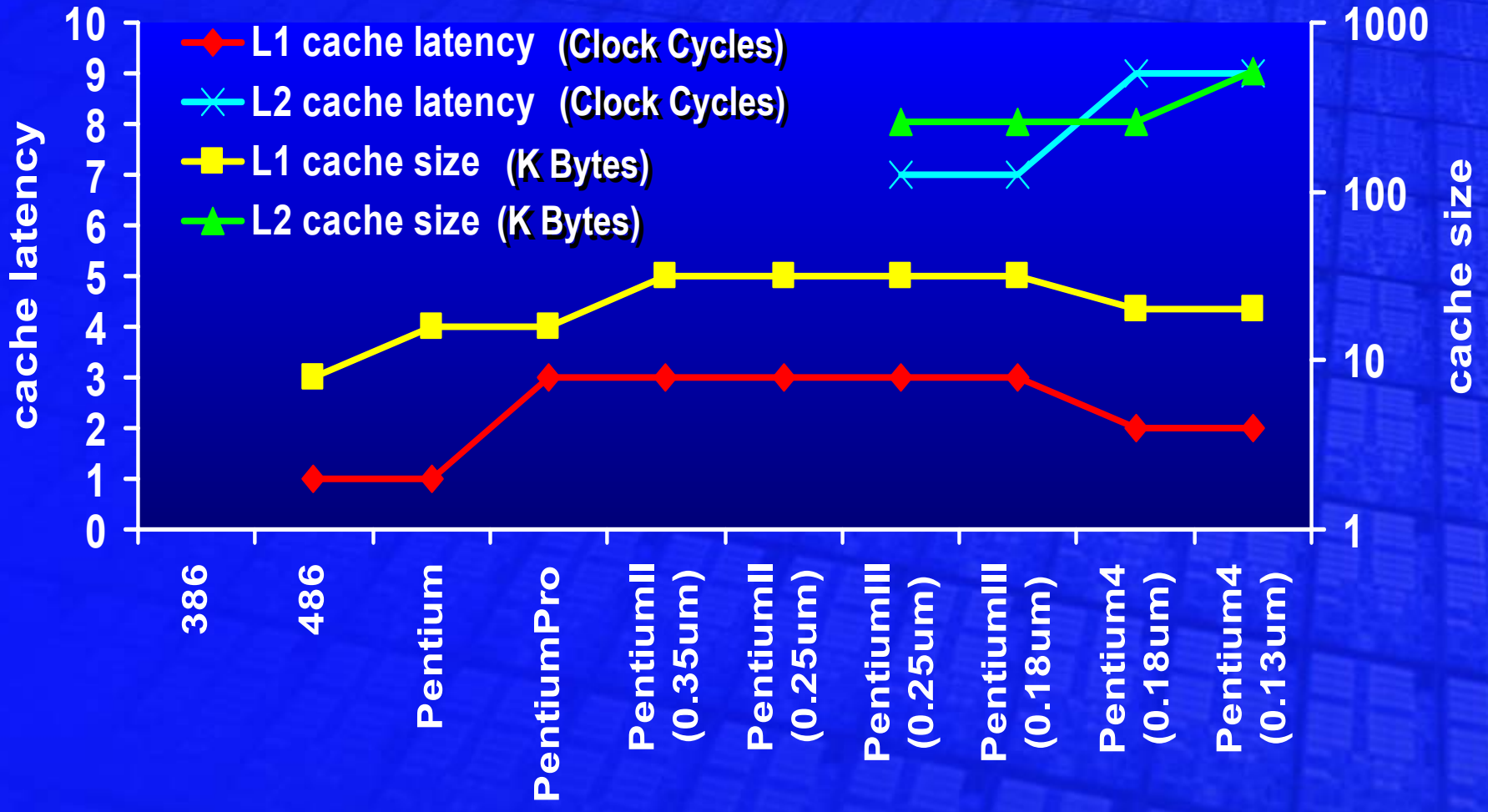


Memory And I/O Bandwidth Are Essential For High Performance

Combating the I/O bottleneck

- Large on chip caches reduce the requirement to go off chip
- Every generation of CMOS scaling increases on chip integration:
  - Reduces need to go off chip
- Advanced circuits to increase the reach of copper
- Advanced packaging keeps high speed components close to each other:
  - Reduces off chip interconnect length
- Optical interconnects for the ultimate in bandwidth, crosstalk and EMI

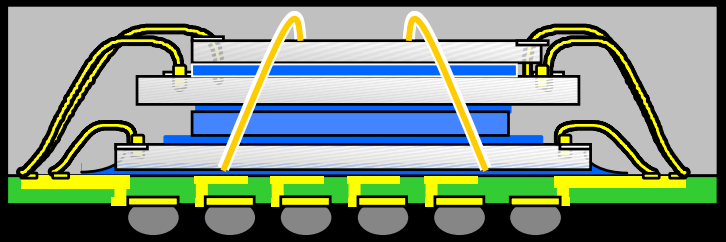
Cache Memory Trend

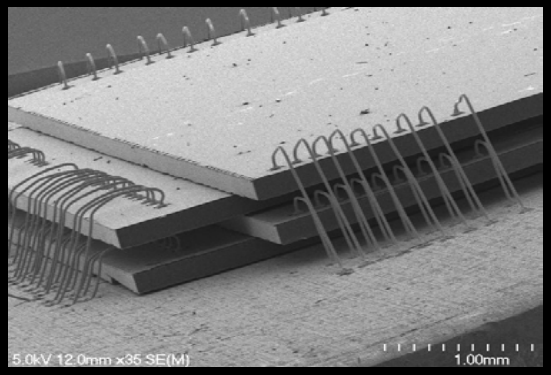


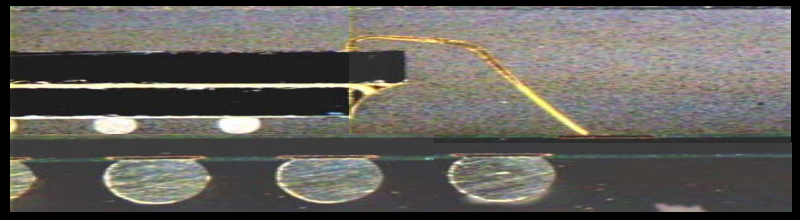
- memory gap
  - Reduce average miss rates
  - Reduce average memory access latency

Integration via Packaging

Wirebond Stacked CSP

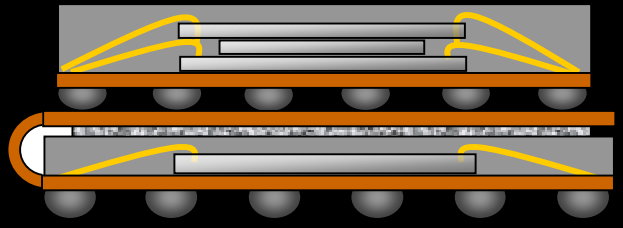


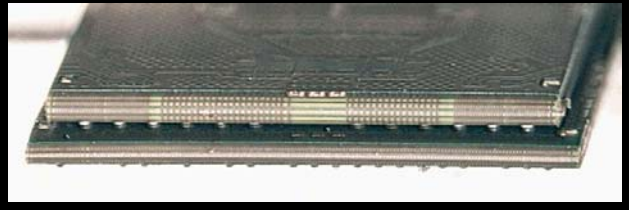




Flip Chip/Wirebond Stacked CSP

Folded Stacked CSP





Advanced packaging keep high speed devices close to each other

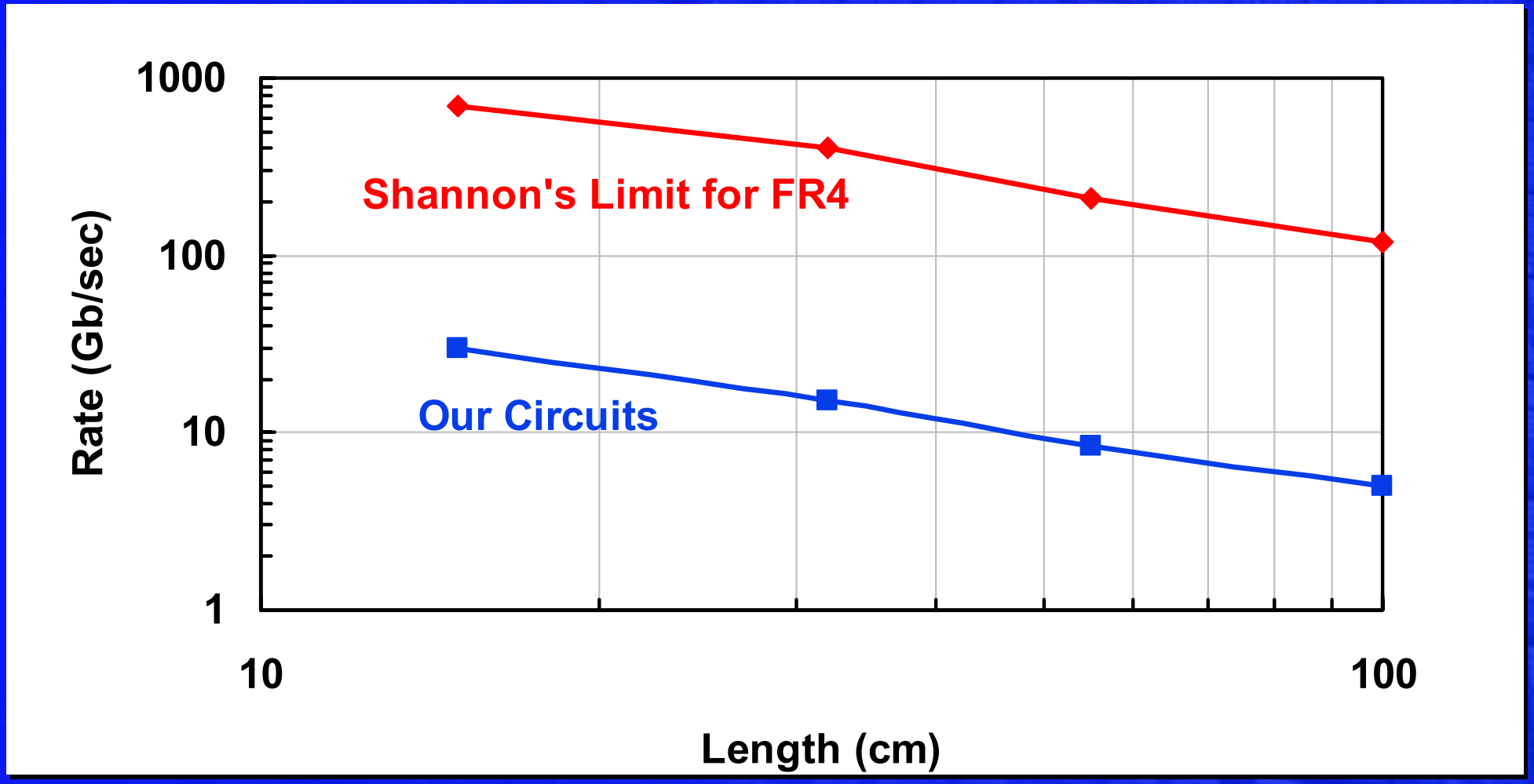
Agenda

- Microprocessor core and I/O speeds
- **Electrical I/O**
- Intel optoelectronics research at universities
- III-V and optical interconnects
- Conclusions
- Backup

Copper for signaling keeps going forward

- Chip-to-chip ~ .25m
- Intra-board ~.5m
- Inter-board ~ 1m
- Box-to-box ~10m
- Advanced circuit techniques
  - **Pre-(distortion/emphasis)/Channel Equalization/High order modulation, etc.**
  - **PCB board material alternative to FR4.**

Copper signaling



- Intel's copper signaling research

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Optoelectronics research

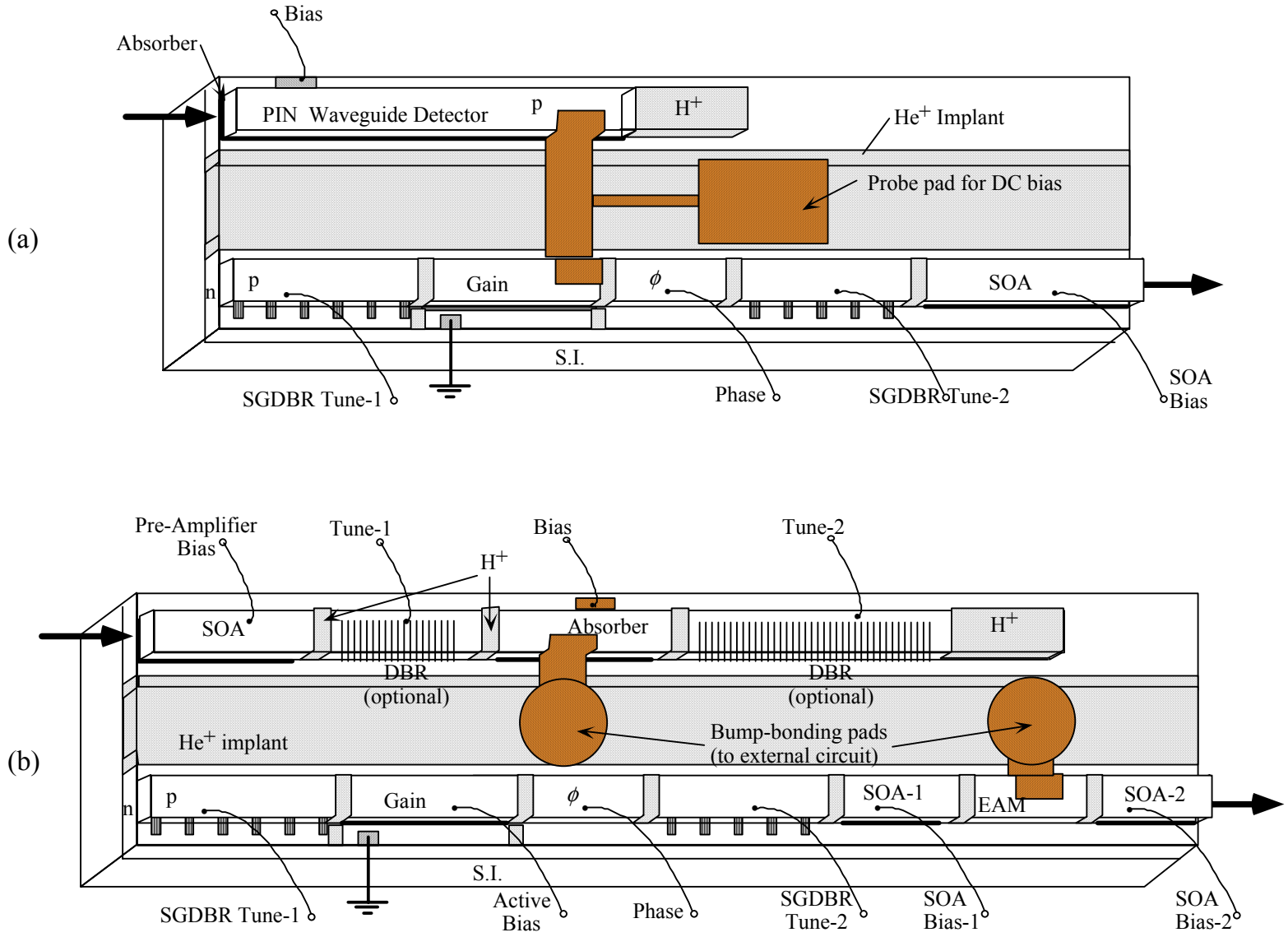
- Will highlight three research projects Intel is sponsoring:
  - UCSB – Prof Larry Coldren
  - Stanford - Prof David Miller
  - Caltech – Prof. Harry Atwater
- Research goals:
  - InP monolithic integration
  - Hybrid integration
  - Silicon nano-crystal research

Overview of UCSB project

John Hutchinson - RIR, George Bourianoff - ARP

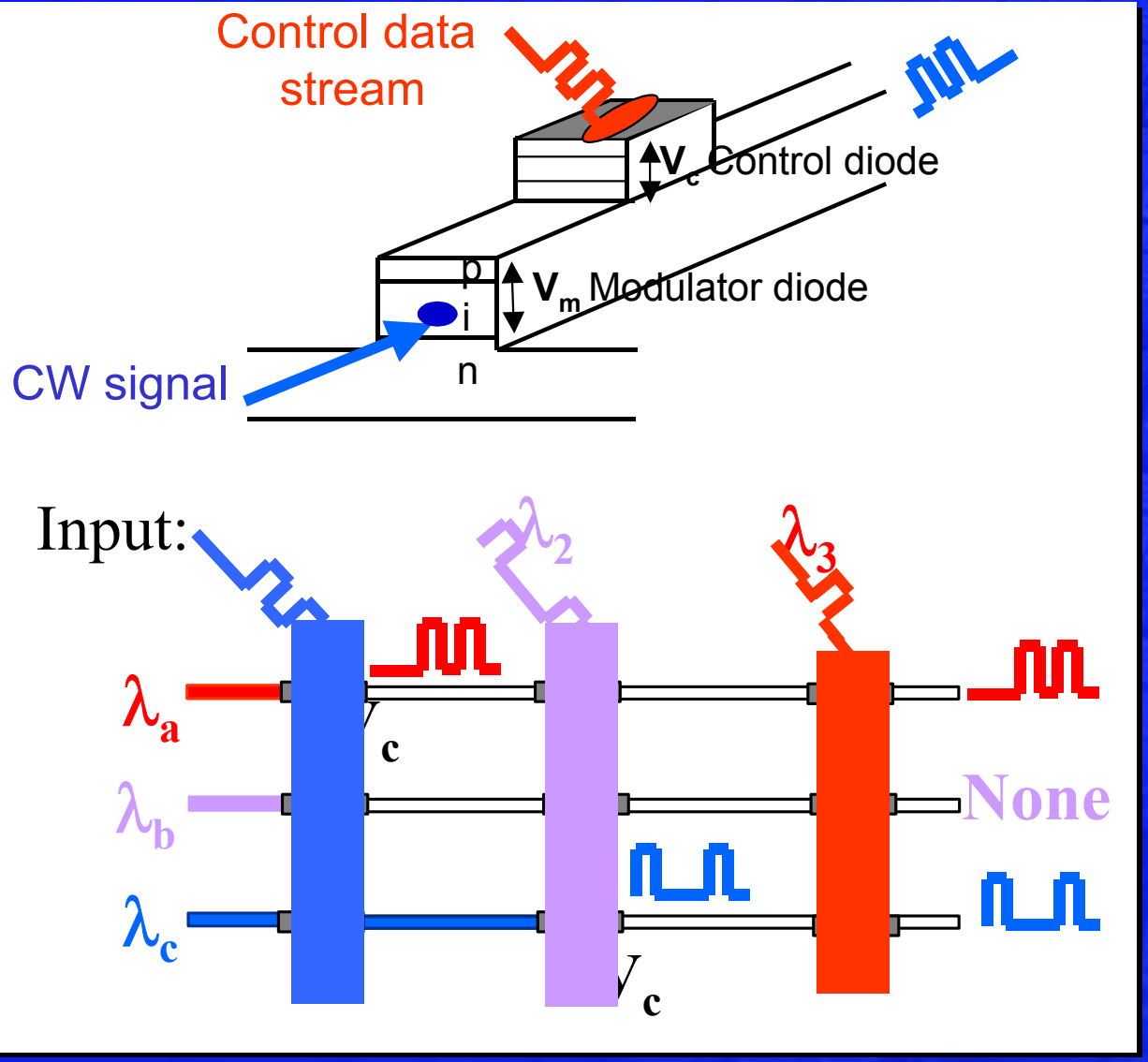
- **Widely tunable wavelength converter: Prof Larry Coldren**
  - **Ridge waveguide platform / PIN diode optical detector**
  - **a) Direct modulation b) Electro-Absorption Modulator**
  - **Widely-tunable SGDBR laser**
  - **Semiconductor Optical Amplifiers**
  - **Heterogeneous device and package integration**
  - **DC, rf testing**

Intel – UCSB research project



- Widely tunable wavelength converter: Prof Larry Coldren

Intel – Stanford Project

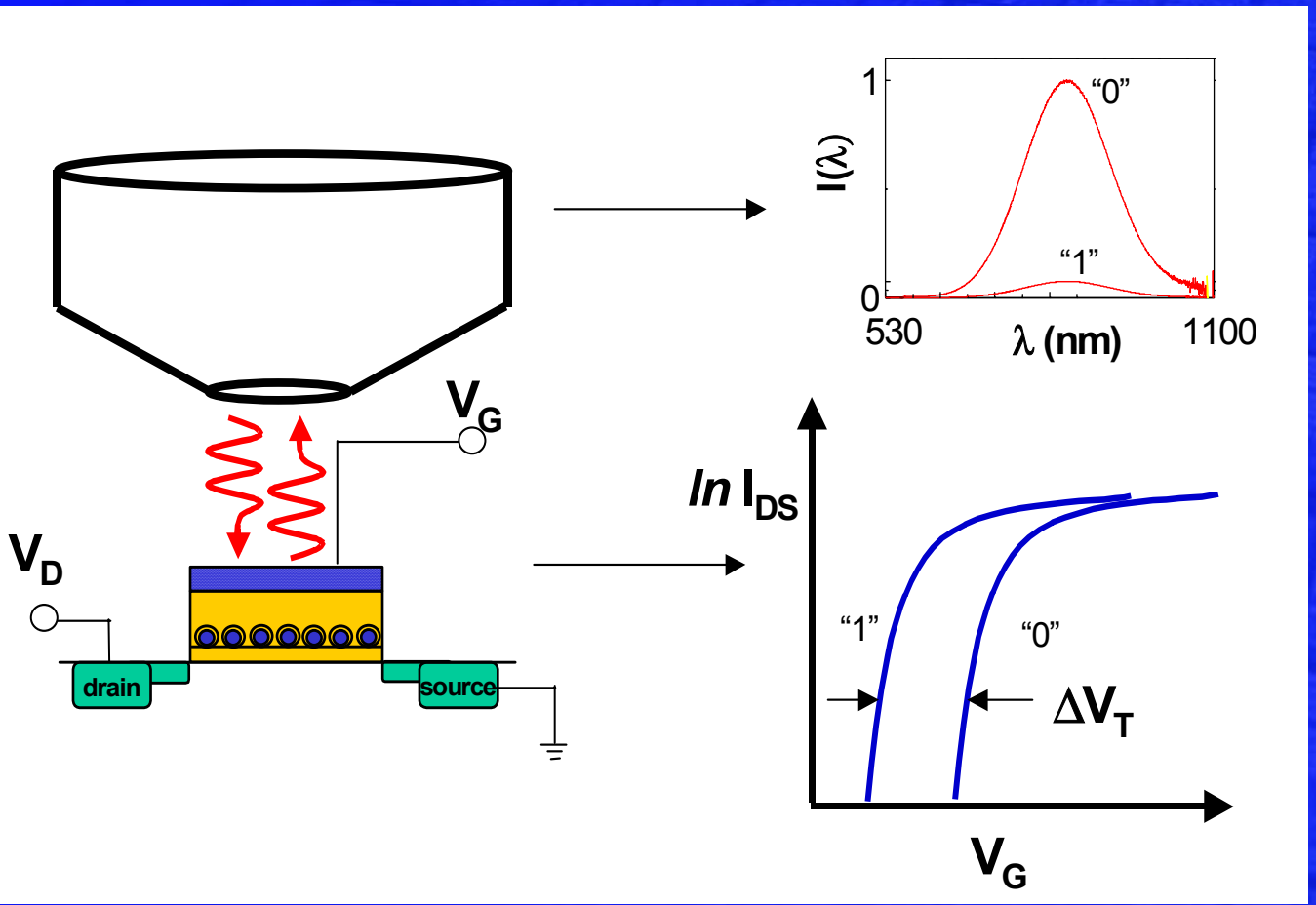


- Evaluate the feasibility of opto-electronic wavelength converters based on integrated quantum well modulator/detector structures for use in 1.5μm optical telecommunications at 40Gb/sec.

Concept for a wavelength converting crossbar switch. Here - two of the switches are enabled using the control voltage.

Prof. David Miller

Overview of Caltech project



- Investigate design and fabrication of all optical memory cell
  - Silicon nano-crystal fabrication
  - Silicon processing at Intel
- Conduct advanced numerical simulation

Concept for an all optical memory cell

With Prof. Harry Atwater

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Opportunities for III-V optoelectronics

PROS

- Virtually unlimited bandwidth:
- No signal crosstalk or EMI
- Latency is about comparable to electrical links

CONS

- High Cost
- Large Form Factor
- Expensive assembly and alignment

Adapting telecom grade optoelectronics to chip to chip Interconnects is an overkill and too costly

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Optoelectronics

- Reinvent III-V optoelectronics technologies developed for telecommunications for mainstream high volume computers:
  - High volume reduces cost of niche components
  - Apply technologies like WDM to improve aggregate data rates:
  - Need low cost Heterogeneous integration techniques
- Need much less focus on loss, high power, dispersion etc as typical link lengths are < 20 inches

Silicon leads in electronic integration and high performance. III-V leads in optoelectronics. In high volume a marriage can only happen if the cost structures and form factors are synchronized

Optical and electronic signaling

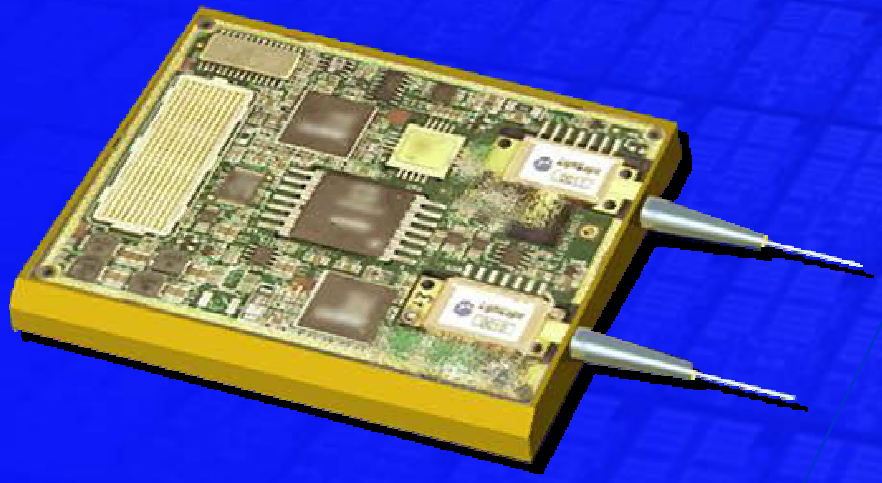
- As bandwidth increase electronic links utilize sophisticated encoding and equalization techniques that can lead to an increase in latency, power and area
- Optical links become attractive if the total cost and form factor of the link is comparable to or less than the total cost of the electrical link

Key Metrics: Bandwidth (with acceptable BER), cost/manufacturability area, power, latency

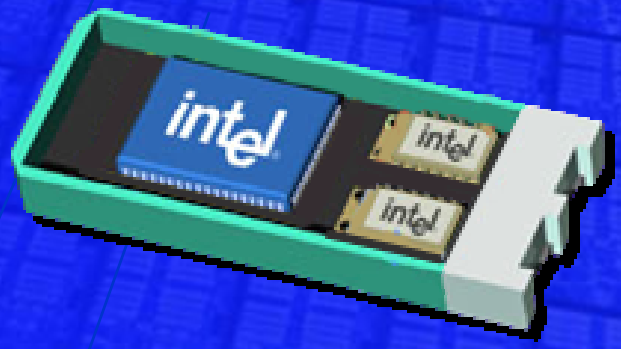
Opportunities for III-V electronics

- Silicon (CMOS, SiGe HBT) will continue to provide the high speed electronics:
  - SiGe is very competitive with InP for speed
- III-V electronics can play a big role if ultra compact monolithic transceivers can be developed specifically for chip to chip I/O at low cost:
  - Every serial I/O link needs two transceivers
  - VCSEL, modulator (if needed), driver, detector and TIA are all integrated onto a monolithic InP substrate

Optical Module Integration for Telecom



Today
10+ Chips
4 Process Technologies



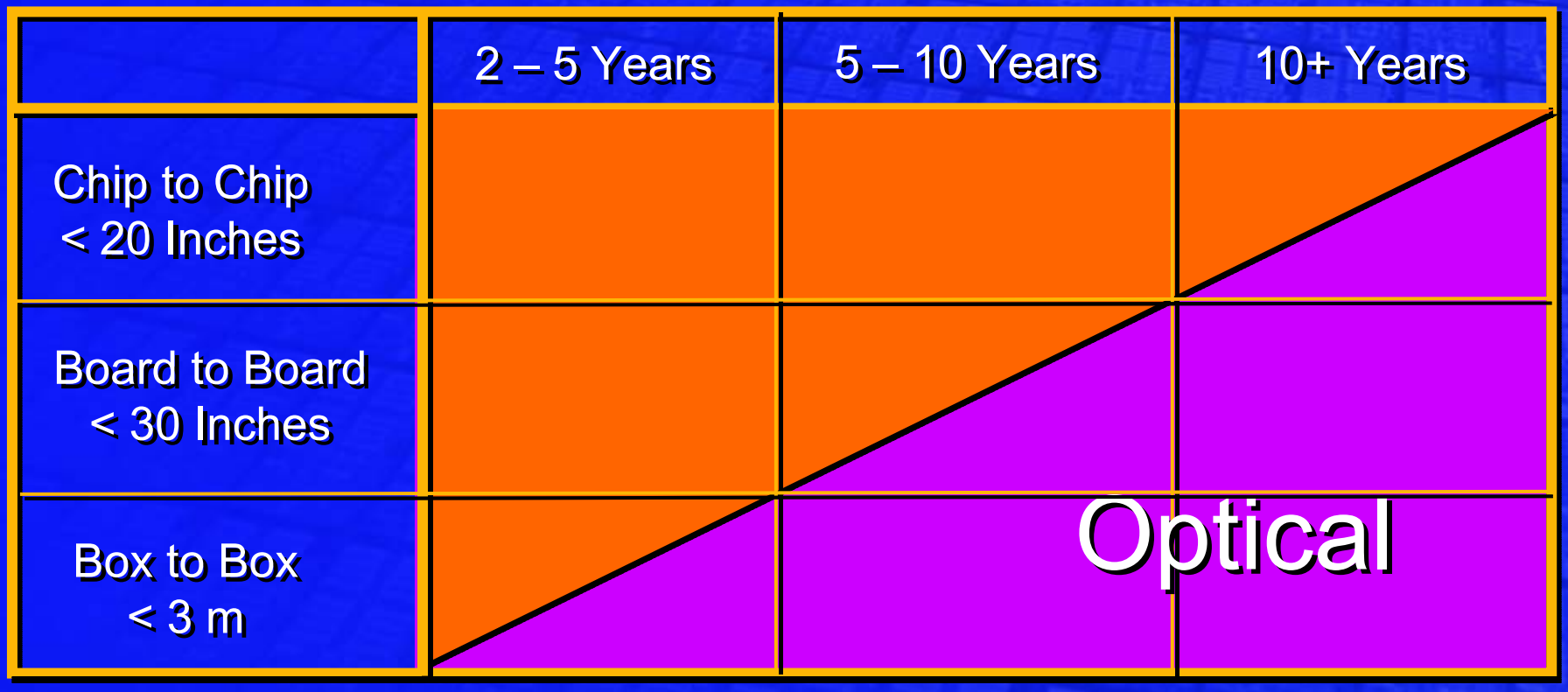
Future (90nm)
3 Chips
2 Process Technologies

4x Cost Reduction
3x Power Reduction

Critical needs

- Area of focus
  - Low cost scalable sources:
    - Direct modulated are desirable
    - External modulators (Polymer/LiNo3, HV vs LV) are OK provided the integration and added drive electronics does not lead to a cost or form factor penalty.
  - High performance detectors
  - Low cost packaging technologies for coupling sources, electronics and detectors
  - High volume manufacturing technologies:
    - Couple sources and detectors either with waveguides or free space links
    - Compatibility with established manufacturing practices

Optical interconnect roadmap as seen today (2002)



- **Copper interconnects are expected to scale in the next 3 – 5 year to 10 Gb/Sec at < 20 inches**

Conclusions

- Copper signaling has the potential to be developed to the 10 – 20 Gb/Sec regime for < 20 inch distances:
  - No physical barriers
  - Advanced circuit techniques
  - New PCB materials
- Optical signaling has great advantages and future potential due to unlimited bandwidth and no crosstalk and EMI:
- For mainstream deployment several factors need to be addressed:
  - Cost must be reduced to be comparable to electrical signaling
    - Address the specific needs of chip to chip interconnects
  - New packaging and integration strategies must be developed
  - Manufacturing techniques must be developed for high volume integration

Acknowledgments

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- Ian Young
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